POLYCRYSTALLINE SILICON OXIDATION METHOD FOR MAKING SHALLOW AND DEEP ISOLATION TRENCHES

FIELD OF THE INVENTION

The invention generally relates to methods for making recessed oxide isolation trenches in semiconductor material for isolating regions of the material from each other.

DESCRIPTION OF THE PRIOR ART

Integrated circuit fabrication usually requires that the individual active and passive circuit elements be electrically isolated from each other in the common semiconductor chip so that desired circuit connections can be made by patterned surface metallization with which the isolated circuit elements are in contact. Many diverse techniques have been proposed, ranging from junction isolation to dielectric isolation, and to combinations thereof, to accomplish the desired isolation. An extensive citation of prior isolation techniques is given in U.S. Pat. No. 4,104,086, issued on Aug. 1, 1978 in the names of James Bondur and Hans Pogge for "Method For Forming Isolated Regions of Silicon Utilizing Reactive Ion Etching" and assigned to the present assignee. U.S. Pat. No. 4,104,086, among other things, cites: (1) U.S. Pat. No. 3,966,577, issued to Arthur Hochberg on June 29, 1976, which discloses a sputter etching method to achieve dielectric isolation using grown or deposited silicon dioxide to fill etched grooves; (2) S. A. Abbas, IBM Technical Disclosure Bulletin, Vol. 20, No. 1, p. 144, June 1977, entitled "Recessed Oxide Isolation Process" which describes a reactive ion etching method to make recessed silicon dioxide filled trenches by partially filling the trenches with evaporated polysilicon material and then oxidizing the material and (3) the paper "A Composite Insulator-Junction Isolation" by R. E. Jones and V. Y. Doo, published in Electrochemical Technology, Vol. 5, No. 5-6, May-June 1967, pages 308-310, which teaches a selective epi process for providing recesses between epi mesas which recesses are filled with oxide and polycrystalline silicon material.

U.S. Pat. No. 4,104,086 itself deals with the problem of avoiding incomplete filling of the isolation trenches with CVD oxide, manifested by an opening or poor quality dielectric region in the center of the CVD filled trenches. The cited problem is avoided by use of tapered walls in the trenches prior to CVD oxide filling. The tapering of the trench walls, however, reduces somewhat device density as a consequence of the corresponding increase in thickness of the CVD oxide-filled trenches at the surface of the semiconductor substrate.

Yet another U.S. Pat. No. 4,139,442, issued on Feb. 13, 1979 to James Bondur and Hans Pogge for "Reactive Ion Etching Method For Producing Deep Dielectric Isolation In Silicon" and assigned to the present assignee, teaches a method for simultaneously making both shallow and deep recessed oxide isolation trenches of equal narrow width where all trenches are filled in simultaneously by thermal oxidation of the vertical walls of the trenches.

SUMMARY OF THE INVENTION

Both shallow and deep recessed oxide isolation trenches are formed in silicon semiconductor substrates partly using a CVD oxide deposition process and partly using a polycrystalline silicon deposition and oxidation process which avoids openings or poor quality dielectric regions in the centers of the filled deep trenches while also avoiding the requirement that the trenches be completely filled by a high temperature process step such as a thermal oxidation step. The shallow trenches may be either narrow or wide but the deep trenches should be narrow so that the deep trenches are filled by a CVD oxide and polycrystalline silicon build-up on the vertical walls of the trenches.

The process comprises reactively ion etching a semiconductor substrate through mask apertures defining narrow, deep trench areas and defining the perimeters of wide, deep trench areas, oxidizing and partially refilling the etched trenches with chemical-vapor-deposited (CVD) oxide, and then completing the filling of the trenches with polycrystalline silicon. The excess polycrystalline silicon covering substrate areas other than the deep trench areas is removed down to the underlying CVD oxide.

The shallow trench areas are etched next, some of the shallow trench areas connecting with the upper regions of the narrow deep trench areas and others of the shallow, trench areas lying inside the perimeters of the wide, deep trench areas. The monocrystalline and polycrystalline silicon in the respective shallow trench areas are removed and the remaining silicon is thermally oxidized.

BRIEF DESCRIPTION OF THE DRAWING

FIGS. **1**, **2**, **3** and **4** are simplified cross-sectional views of the structure obtaining at successive times during the fabrication of shallow and deep recessed oxide isolation trenches formed in silicon semiconductor substrates in accordance with the process of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

The structure of FIG. **1** includes monocrystalline silicon substrate **10** which is shown as P^- conductivity for illustration purposes, an N^+ layer **12** over the substrate **10** and an N^- conductivity layer **14** on the layer **12**. For the purposes of the invention, either all or some of the layers **10**, **12** and **14** could be of opposite conductivity type from the conductivity types indicated. However, it is preferred that layer **12** be of high conductivity where it later becomes the collector of a bipolar transistor.

The structure of FIG. **1** can be fabricated by various techniques. The preferred technique, however, is to provide a P^- monocrystalline silicon substrate **10** and to diffuse an N^+ blanket diffusion into the substrate (to produce region **12**) by using conventional diffusion or ion implantation of an N-type impurity such as arsenic, antimony or phosphorous to produce an N^+ region with a surface concentration of between about 1×10^{19} or 1×10^{21} atoms/cc. The layer **14** is subsequently grown over layer **12** by means of epitaxial growth. This may be done by conventional techniques such as by the use of Si Cl_4/H_2 or Si H_4/H_2 mixtures at growth temperatures of about 1,000° C. to 1,200° C. The N^+ layer may have a typical thickness of between 1-3 microns whereas the epitaxial layer may have a thickness of from 0.5 to 10 microns, the exact thicknesses depending upon the device to be built.

Alternatively, the structure could be made by various combinations of thermal diffusion, ion implantation